IN THE CLAIMS:

Claims 1-26 have been canceled.

1. (new): An electronic circuit having

an input for inputting at least one information signal;

an energy means for converting energy contained in the at least one information signal into a voltage supply;

a control means for generating at least one switch-on control signal when an information signal arrives; and

a signal processing means for storing an information item represented by the at least one information signal and/or for evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop;

wherein the signal processing means can be activated by the at least one switch-on control signal for the purpose of evaluation and/or storage;

and wherein, during the evaluation and/or storage, the at least one information signal may be the sole energy source for the electronic circuit;

wherein the at least one switch-on control signal has the following signals;

an activation signal for activating precharge transistors of the at least one ferroelectric flip-flop;

transfer signal for transferring the information contained in ferroelectric capacitors of the at least one ferroelectric flip-flop onto internal data lines of the at least one ferroelectric flip-flop; and

a current switching signal for switching on the voltage supply of the signal processing means.

2. (new): The electronic circuit as claimed in claim 1, wherein the control means can generate at least one switch-off control signal after a predetermined time has elapsed after the at least one information signal arise and when the energy converted from the at least one information signal is exhausted,

wherein the signal processing means can be caused or is caused to effect a storage and to effect deactivation by the at least one switch-off control signal.

3. (new): The electronic circuit as claimed in claim 1 or 2, wherein the information stored in the at least one ferroelectric flip-flop can be converted into at least one output signal by the signal processing means and the electronic circuit furthermore has at least one output for outputting the at least one output signal.

4. (new): The electronic circuit as claimed in claim 1, wherein the electronic circuit furthermore has a display means for displaying the information stored in the at least one ferroelectric flip-flop.

5. (new): The electronic circuit as claimed in claim 4, wherein the display means is concomitantly supplied by the voltage supply generated by the energy means.

6. (new): The electronic circuit as claimed in claim 4 or 5, wherein the display means has an LCD display.

7. (new): The electronic circuit as claimed in claim 3, wherein an external voltage supply and external control means can be connected for the outputting of the information stored in the at least one ferroelectric flip-flop by the signal processing means.

8. (new): The electronic circuit as claimed in claim 2, wherein the at least one switch-off control signal has the following signals:

a transfer end signal;

an activation signal for activating precharge transistors of at least one ferroelectric flip-flop; and

a current switch-off signal for switching off the voltage supply of the signal processing means.

9. (new): The electronic circuit as claimed in claim 1, wherein signal lines for each of the switch-on signals lead from the control means to the signal processing means.

10. (new): The electronic circuit as claimed in claim 8 or 9, wherein signal lines for each of the switch-off signals lead from the control means to the signal processing means.

11. (new): The electronic circuit as claimed in claim 10, wherein, for the transfer signal and the transfer end signal, a common transfer signal line leads from the control means to the signal processing means, the transfer signal consists in the application of a voltage to the common transfer signal line and the transfer end signal consists in the disconnection of the voltage on the common transfer signal line.

12. (new): The electronic circuit as claimed in claim 10, wherein, for the current switching signal and the current switch-off signal, a common current signal line leads from the control means to the signal processing means, the current switching signal consists in the application of a voltage to the common current signal line and the current switch-off signal consists in the disconnection of the voltage on the common current signal line.

13. (new): The electronic circuit as claimed in claim 1, wherein the signal processing circuit is a counting circuit for evaluating a plurality of information signals, which arrive successively or simultaneously by counting the information signals that have arrived.

14. (new): The electronic circuit as claimed in claim 13, wherein the counting circuit comprises a plurality of cascaded edge-controlled ferroelectric flip-flops, in which the at least one information signal is input into the clock input of the first ferroelectric flip-flop of the plurality of cascaded ferroelectric flip-flops and the output of each of the ferroelectric flip-flops, except for the last, is in each case also connected to the clock input of the ferroelectric flip-flop connected downstream.

15. (new): A method for storing information represented by at least one information signal or information obtained through evaluation of the at least one information signal in at least one ferroelectric flip-flop in a signal processing means, having the following steps:

A: generating at least one switch-on control signal from an information signal that has arrived, and generating a voltage supply from energy contained in the at least one information signal;

B: activating the signal processing means by the switch-on control signal and applying the voltage supply to the signal processing means, wherein step B has the sub-steps:

B1: activating precharge transiftors of the at least one ferroelectric flip-flop by applying a voltage;

B2: deactivating the precharge transistors of the at least one ferroelectric flip-flop by disconnecting the voltage;

B3: applying a voltage to ferroelectric capcitors of the at least one ferroelectric flip-flop for transferring the information stored in the ferroelectric capacitors to logic gate of the at least one ferroelectric flip-flop; and

B4: activating the voltage supply of the logic gates of the at least one ferroelectric flip-flop;

C: storing an information item represented by the at least one information signal and/or evaluating an information item represented by the at least one information signal and storing the secondary information obtained through the evaluation by means of at least one ferroelectric flip-flop;

D: generating a switch-off control signal after a predetermined time has elapsed after the at least one information signal arrives and/or when the energy converted from the at least one information signal is exhausted; and

E: deactivating the signal processing means by the switch-off control signal.

16. (new): The method as claimed in claim 15, wherein step E has the sub-steps:

E1: disconnecting a voltage present across ferroelectric capacitors of the at least one ferroelectric flip-flop;

E2: deactivating the voltage supply of the logic gates of the at least one ferroelectric flip-flop;

E3: activating precharge transistors of the at least one ferroelectric flip-flop by applying a voltage; and

E4: deactivating the precharge transistors of the at least one ferroelectric flip-flop by disconnecting the voltage.

17. (new): The method as claimed in one of claims 15 or 16, wherein the electronic circuit contains a plurality of ferroelectric flip-flops and the evaluation comprises a summation of the value represented by the information signal and a value already stored in the ferroelectric flip-flops.

18. (new): The method as claimed in claim 17, wherein the summation is effected by means of a counting operation, in which plurality of ferroelectric flip-flops are cascaded in a counter arrangement and an arriving information signal increments or decrements a counter reading of the counter arrangement by the value 1.

19. (new): The method as claimed in claim 15, wherein the information stored in the at least one ferroelectric flip-flop can be converted into at least one output signal and be output from the electronic circuit.

RESPONSE

Claims 1-26 are pending. The Examiner objects to Claims 5,6,8-15 and 17-20. The Examiner rejects Claims 1-4, 7, 16 and 21-26.

Accordingly, applicant herewith cancels claims 1-26 and submits new claims 1-19 to overcome the objections and rejections. The amendments add no new matter.

The examiner rejected claims 22-26 under 35 U.S.C. 101 as unsupported by either a specific asserted utility or well established utility and under 35 U.S.C. 112, first paragraph. Applicants respectfully traverse this rejection.

Applicant cancels herewith original claims 22-26. Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection of claims 22-26 under 35 U.S.C. 101.

The Examiner rejects claims 1-4, 7, 16, 21, 22 and 25 under 35 U.S.C. 103(a) as being unpatentable over Eschmann et al (EP 549,519 A1) in view of Ooms et al. (US 5,923,184. Applicants respectfully traverse this rejection.

A reference or a combination of references must teach or suggest all elements of a claim to render the claim obvious. Neither Eschmann nor Ooms teaches or suggests the realization of the switch-on signal or of the advantageous effects resulting therefrom as the present invention discloses and claims.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejection of claims 1-4, 7, 16, 21, 22 and 25 under 35 U.S.C. 103(a) as being unpatentable over Eschmann in view of Ooms.

In view of Applicant's amendments and remarks, the specifications and claims are believed to be in condition for allowance. Reconsideration, withdrawal of the rejections, and passage of the case to issue is respectfully requested. If any fees not accounted for above are due in connection with the filing of this paper, please charge the fees to our Deposit Account No. 02-3732.

Respectfully submitted,

Date: 12/3/03

By _____
Jeffrey R. Stone (Reg. No. 47,976)
Briggs and Morgan, P.A.
2200 IDS Center
80 South Eighth Street
Minneapolis, MN 55402
Telephone: (612) 977-8560